IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

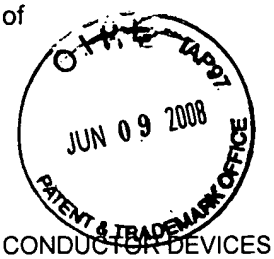
In re Patent Application of

PHILLIPS et al.

Serial No. 10/577,938

Filed: May 3, 2006

Title: STRAINED SEMICONDUCTOR DEVICES



Atty Dkt. SCS-124-1158
C# M#
Confirmation No. 5737
TC/A.U.: 2814
Examiner: H. Weiss
Date: June 9, 2008

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

☐ **Correspondence Address Indication Form Attached.**

☐ **NOTICE OF APPEAL**
Applicant hereby **appeals** to the Board of Patent Appeals and Interferences from the last decision of the Examiner twice/finally rejecting applicant's claim(s). $510.00 (1401)/$255.00 (2401) $

☒ An appeal **BRIEF** is attached in the pending appeal of the above-identified application $510.00 (1402)/$255.00 (2402) $ 510.00

☐ Credit for fees paid in prior appeal without decision on merits -$ ( )

☐ A reply brief is attached. **(no fee)**

☐ Petition is hereby made to extend the current due date so as to cover the filing date of this paper and attachment(s)
One Month Extension $120.00 (1251)/$60.00 (2251)
Two Month Extensions $460.00 (1252)/$230.00 (2252)
Three Month Extensions $1050.00 (1253/$525.00 (2253)
Four Month Extensions $1640.00 (1254/$820.00 (2254) $

☐ "Small entity" statement attached.

Less month extension previously paid on -$( )

TOTAL FEE ENCLOSED $ 510.00

☒ **CREDIT CARD PAYMENT FORM ATTACHED.**

Any future submission requiring an extension of time is hereby stated to include a petition for such time extension. The Commissioner is hereby authorized to charge any deficiency, or credit any overpayment, in the fee(s) filed, or asserted to be filed, or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our **Account No. 14-1140.** A duplicate copy of this sheet is attached.

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NIXON & VANDERHYE P.C.
By Atty: Stanley C. Spooner, Reg. No. 27,393

Signature: _____

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of	Confirmation No.: 5737
PHILLIPS et al.	Atty. Ref.: 124-1158
Serial No. 10/577,938	Group: 2814
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For: STRAINED SEMICONDUCTOR DEVICES

* *

APPEAL BRIEF

On Appeal From Group Art Unit 2814

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APPEAL BRIEF

Sir:

I. REAL PARTY IN INTEREST

The real party in interest in the above-identified appeal is QinetiQ Limited by virtue of an assignment of rights from the inventors to QinetiQ Limited recorded May 3, 2006 at Reel 17893, Frame 535.

II. RELATED APPEALS AND INTERFERENCES

There are believed to be no related appeals, interferences or judicial proceedings with respect to the present application, other than the Pre-Appeal Brief Request for Review previously filed in this appeal on March 31, 2008.

III. STATUS OF CLAIMS

Claims 1-14 and 16 stand rejected in the second non-final Official Action and claim 15 has previously been cancelled without prejudice. The Examiner contends that claims 9 and 16 are rejectable under 35 USC §112 (first paragraph) as failing to comply with the written description requirement. The Examiner also contends that claims 1-9, 12-14 and 16 are anticipated under 35 USC §102 by Phillips '674 (WO 03/081674). The Examiner additionally contends that claims 1, 10 and 11 are anticipated under 35 USC §102 by Phillips '337 (WO 01/93337). The above rejections of claims 1-14 and 16 are appealed.

IV. STATUS OF AMENDMENTS

No further response has been submitted with respect to the second non-final Official Action in this application other than the filing of a Pre-Appeal Brief Request for Review which Panel decision was mailed May 7, 2008 (Paper No. 20080506).

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

Appellants' specification and figures provide an explanation of the claimed invention set out in independent claims 1 and 16, with each claimed structure addressed as to its location in the specification and in the figures.

1. A transistor [as shown in Figures 1 and 4 and discussed at page 4, line 26 to page 5, line 17 and page 5, line 22 to page 6, line 21 and elsewhere in the specification] including at least one narrow bandgap region [layer 5 shown in Figure 1 and discussed on page 4, line 27 to page 5, line 1, layer 19 shown in figure 4 and discussed on page 6, lines 9-11 and elsewhere in the specification] under compressive mechanical strain [Figure 1 embodiment discussed on page 5, lines 8-10 and Figure 4 embodiment discussed on page 6, lines 9-11 and elsewhere in the specification] comprising at least one of a doped p-type material [layer 5 shown in Figure 1 and discussed on page 4, line27 to page 5, line 1, layer 19 shown in figure 4 and discussed on page 6, lines 1-2 and elsewhere in the specification] and a material containing an excess of holes [holes introduced by modulation doping of layer 5 shown in Figure 1 and discussed on page 4, line 28 and page 5, lines 1-2 and elsewhere in the specification].

16. A quantum-well field effect transistor [as shown in Figure 1 and discussed at page 4, line 26 to page 5, line 17 and page 5, lines 22-29 and elsewhere in the specification] including at least one narrow bandgap region [layer 5 shown in Figure 1 and discussed on page 4, line27 to page 5, line 1 and elsewhere in the specification] or layer that is doped p-type [layer 5 shown in Figure 1 and discussed on page 4, line 28 and elsewhere in the specification] or contains an excess of holes [the modulation doping of layer 5 shown in Figure 1

and discussed on page 4, line 28 to page 5, line 2 and elsewhere in the specification] and is subject to compressive mechanical strain [Figure 1 embodiment discussed on page 5, lines 8-10 and elsewhere in the specification], wherein said transistor incorporating a conducting region consisting at least partly of a quantum well [layer 5 shown in Figure 1 and discussed on page 4, line 28 to page 5, line 1 and elsewhere in the specification]; (b) the quantum well is in an at least partly intrinsic conduction regime when the transistor is unbiased and at a normal operating temperature [requirements as discussed on page 3, lines 4-11 and elsewhere in the specification]; and (c) it includes at least one junction which is biasable to reduce the intrinsic conduction in the quantum well and confine charge carriers predominantly to one type only corresponding to an extrinsic saturated regime [the junction between layers 4 and 5 and/or the junction between layers 5 and 6 as shown in Figure 1].

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 9 and 16 stand rejected under 35 USC §112 (first paragraph) as failing to comply with the written description requirement.

Claims 1-9, 12-14 and 16 stand rejected under 35 USC §102(b) as being anticipated by Phillips '674 (WO 03/081674).

Claims 1, 10 and 11 stand rejected under 35 USC §102(b) as being anticipated by Phillips '337 (WO 01/93337).

VII. ARGUMENT

Appellants' arguments include the fact that the burden is on the Examiner to first and foremost properly construe the language of the claims to determine what structure and/or method steps are covered by that claim. After proper construction of the claim language, the burden is also on the Examiner to demonstrate where a single reference (in the case of anticipation) teaches each of the structures recited in independent claims 1 and 16.

The Court of Appeals for the Federal Circuit has noted in the case of *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick*, 221 USPQ 481, 485 (Fed. Cir. 1984) that "[a]nticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim."

A. The rejection of claims 9 and 16 under 35 USC §112 (first paragraph) is not supported by the facts – the Examiner fails to appreciate that the alleged missing written description is disclosed in Appellants' specification, is known by those of ordinary skill and is present in previously published prior art

The Examiner alleges in the rejection under §112 that the present specification

> does not contain a description/depiction of the quantum well being in at least partly intrinsic conduction regime when the transistor is unbiased and at normal operation temperature and at least one

> junction which is bistable to reduce the intrinsic conduction and confine charge carriers.

The Examiner's attention is directed to the fact of Appellants' originally filed specification, page 3, lines 4-11 which has almost literal correspondence with the subject matter of claims 9 and 16, i.e., the specification states

> (b) the quantum well is in an at least partly intrinsic conduction regime when the transistor is unbiased and at a normal operating temperature; and (c) it includes at least one junction which is biasable to reduce the intrinsic conduction in the quantum well and confine charge carriers predominantly to one type only corresponding to an extrinsic saturated regime.

The fact is that the originally filed specification has a written description as included in claim 9 and 16 and clearly points out that this information is disclosed in UK Patent Application Serial No. 2 362 506 which was published November 21, 2001 (prior to filing the application). Appellants' specification merely restates that which is known in the art in view of this publication long prior to the present application's priority date of November 20, 2003.

It is also noted that the inventor of GB 2 362 506 is a co-inventor of the present application which is an improvement on this previous publication. The current inventors found the unobvious benefit in placing the transistor's narrow bandgap region "under compressive mechanical strain." That improvement is not disclosed in the earlier GB patent. It is noted that the Examiner makes no allegation that that improvement (recited in independent claims 1 and 16) is not fully supported in the present application.

Thus, with respect to the first paragraph of §112 requirement of a written description, an almost literal written description is in the present specification and is disclosed in the noted prior art. Accordingly, the question is, did the inventor at the time the application was filed, "have" possession of the claimed invention. Because of the literal correspondence between the subject matter of claim 9 as well as the corresponding subject matter of claim 16 in Appellants' specification page 3, lines 5-11, Appellants clearly had possession of this aspect of the claimed invention when the application was filed.

The Examiner also raises a new argument in the second non-final Official Action suggesting that the specification fails to contain a description of "at least one junction which is bistable to reduce the intrinsic conduction and confine charge carriers." It is suspected that this reference is a typographical error in the Official Action, as there is no reference in claims 9 or 16 to a "bistable" junction.

It is noted that claims 9 and 16 instead reference "at least one junction which is biasable . . . ." As noted above, Appellants' specification, page 3, lines 4-11, contains a discussion of UK Patent Application 2 362 506 which was published November 21, 2001. Appellants' specification notes that in the prior UK patent application, there is a clear disclosure relating to an extracting transistor which includes "at least one junction which is biasable to reduce the intrinsic conduction in the quantum well and confine charge carriers predominantly to one type only

corresponding to an extrinsic saturated regime" which is the exact language of Appellants' claims 9 and 16.

Quite clearly, the subject matter limitations of claims 9 and 16 by themselves were clearly in the public domain at the time of filing the present application, although those claims depend from or incorporate the improvement which is included in the subject matter of the independent claims, i.e., material which is "subject to compressive mechanical strain." This inventive aspect, in combination with the features of claims 9 and 16, was not in the public domain, nor was there any recognition of the beneficial effects of this combination of elements. A copy of GB 2 362 506 is attached hereto in the Evidence Appendix.

While it is possible that the Examiner may have overlooked this portion of Applicants' specification, the recited portion of the specification clearly meets the "written description" requirements of §112 (first paragraph) with respect to claims 9 and 16 and any further rejection thereunder is respectfully traversed.

B. The Examiner fails to establish where Phillips '674 contains any disclosure of "at least one narrow bandgap region under compressive mechanical strain" as required by independent claims 1 and 16

While the Examiner generally alleges, in the paragraph bridging the official action pages 2 and 3, that Phillips '674 shows the provision of "compressive mechanical strain," he fails to identify any such teaching in the reference.

In fact, the Examiner suggests that page 10, lines 21 and 22 of Phillips '674 has to do with "providing compressive mechanical strain" when the cited portion of Phillips '674 actually states "[i]t should be noted that in all cases the layers are nominally undoped, but may contain unintentional doping of either type." This language has **nothing** to do with **any** mechanical straining of **any** layer, let alone **compressive** strain of **the narrow bandgap region**.

There is no disclosure in Phillips '674 that there is any doping which would inherently provide "at least one narrow bandgap region under compressive mechanical strain." Again, should the Examiner persist in this unfounded allegation, he is respectfully requested to indicate specifically where any such teaching exists in the Phillips '674 reference.

It is possible that, because the Phillips '674 combination of elements is similar to the combination of elements set out in the present specification, the Examiner may believe that "compressive mechanical strain" is somehow inherently disclosed in Phillips '674. However, as discussed in the present specification on pages 4-5 variations in the layer thicknesses as well as the differing lattice constants of the materials **can** be combined to provide different types of mechanical strain (both compressive and tensile), but no recognized that "compressive mechanical strain" would have the disclosed beneficial effect.

Additionally, pages 5 and 6 disclose an embodiment shown in Figure 3 which has the appropriate materials and thicknesses to provide "light hole

transport and permitting faster device speed with lower base access resistance for improved power gain." There is simply no recognition in the prior art that providing the claimed "compressive mechanical strain" has any beneficial effect and the Appellants discovery is a significant improvement in the arts.

Absent any teaching in the Phillips '674 reference of "compressive mechanical strain" in the recited transistor components, the anticipation rejection clearly fails.

Moreover, Phillips '674 actually "teaches away" from the claimed invention because it teaches "a structure that is strain balanced . . . ." A "strain balanced" structure is not a structure "under compressive mechanical strain" but rather one in which the lattice constants and thicknesses of the layers is chosen such that lattice strain is balanced, i.e., no strain.

As a result, the independent claims 1 and 16 would not even be obvious in view of Phillips '674 since it would lead one of ordinary skill in the art towards "strain balance" and away from the claimed combination of elements and interrelationships (including "compressive mechanical strain").

Accordingly, the Examiner has simply failed to meet his burden of establishing a *prima facie* case of anticipation of claims 1 and 16 or claims dependent therefrom in view of the Phillips '674 reference.

C. The Examiner fails to even allege that Phillips '337 contains any suggestion of "at least one narrow bandgap region under compressive mechanical strain"

With Phillips '674, the Examiner alleges that there is a disclosure of "compressive mechanical strain" and merely fails to identify where that disclosure exists in the Phillips '674 patent (and as noted above, this clearly does not exist in Phillips '674). With reference to the Phillips '337 patent, the Examiner does not even allege that the reference has any teaching of the claimed bandgap region "under compressive mechanical strain."

Nowhere in section 5 of the second non-final rejection is there any allegation that Phillips '337 teaches any structure "under compressive mechanical strain," e.g.,

> "Phillips '337 show [sic] all aspects of the instant invention 9e.g. Figure 1) including a NPN transistor 10 with a P-type material base region 21 with a base contact 24, emitter 36 and collector 16 arranged as claimed and having bandgap greater than 0.e eV and doping level gre3ater [sic] than 10^{17} cm^{-3}."

Without even an allegation that Phillips '337 discloses the "under compressive mechanical strain" interrelationships clearly set out in Applicants' independent claims 1 and 16, the anticipation rejection of independent claim 1 over Phillips '337 is simply incorrect and comprises reversible error.

D. There is no basis for any future obviousness rejection over Phillips '674 and/or Phillips '337

To the extent the Examiner may contend that independent claims 1 and 16 recite structure and structural combinations which would be obvious in view of either Phillips '674 or Phillips '337, it should be noted that the provisions of 35 USC §103(c) may apply, in that these two references were owned by the same person or subject to an obligation of assignment to the same person, i.e., QinetiQ Limited, the assignee of the current application.

Moreover, even if §103(c) were not appropriate, there is either no disclosure of "compressive mechanical strain" (in Phillips '337) and a specific teaching away from "compressive mechanical strain" (in Phillips '674's teaching of "strain balance"), and accordingly any rejection under 35 USC §103 would clearly fail.

E. The Examiner fails to establish that all elements in claims 1-9, 12-14 and 16 are disclosed in Phillips '674

As noted above in section B, the Examiner has simply failed to identify any portion of Phillips '674 which discloses "at least one narrow bandgap region under compressive mechanical strain" as required in both independent claims 1 and 16. As per the *Lindemann* case above, the Examiner has failed to demonstrate where or how every claimed element and every claimed interrelationship is disclosed in the Phillips '674 reference.

Accordingly, while the burden is on the Examiner to establish where the prior art teaches the claimed elements, he has failed to meet this burden and has not set out any *prima facie* case of anticipation under 35 USC §102(b) and therefore the rejection of claims 1-9, 12-14 and 16 is unsupported and is respectfully traversed.

F. The Examiner fails to establish that all elements in claims 1, 10 and 11 are disclosed in Phillips '337

As noted above in section C, the Examiner has simply failed to identify any portion of Phillips '337 which discloses "at least one narrow bandgap region under compressive mechanical strain" as required in claims 1, 10 and 11. Accordingly, as per the *Lindemann* case above, the Examiner has failed to demonstrate where or how every claimed element and every claimed interrelationship is disclosed in the Phillips '337 reference.

Accordingly, while the burden is on the Examiner to establish where the prior art teaches the claimed elements, he has failed to meet this burden and has not set out any *prima facie* case of anticipation under 35 USC §102(b) and therefore the rejection of claims 1, 10 and 11 is unsupported and is respectfully traversed.

VIII. CONCLUSION

A brief review of Appellants' specification on page 3, lines 4-11 will show literal written description for the limitation recited in claims 9 and 16 and therefore Appellants completely complies with the §112 (first paragraph) requirement of a written description in the specification. Neither the Phillips '674 patent nor the Phillips '337 patent contains any disclosure of "at least one narrow bandgap region under compressive mechanical strain." Thus, because all claimed elements and structural interrelationships **are not shown in a single prior art reference**, there is no basis for an "anticipation" rejection. In fact, because Phillips '674 teaches "strain balance," it would lead one of ordinary skill in the art away from Appellants' claimed combination of elements.

As a result of the above, there is simply no support for the rejections of Appellants' independent claims or claims dependent thereon under 35 USC §112 or §102. Thus, and in view of the above, the rejection of claims 1-14 and 16 under 35 USC §§112 and 102 is clearly in error and reversal thereof by this Honorable Board is respectfully requested.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: _____

Stanley C. Spooner
Reg. No. 27,393

SCS:kmm
Enclosure

IX. CLAIMS APPENDIX

1. A transistor including at least one narrow bandgap region under compressive mechanical strain comprising at least one of a doped p-type material and a material containing an excess of holes.

2. A transistor according to claim 1 wherein said narrow bandgap region is arranged for majority carrier transport.

3. A transistor according to claim 1 wherein said narrow bandgap region is in contact with at least one layer having a different lattice constant whereby said narrow bandgap region is subject to said compressive mechanical strain.

4. A transistor according to claim 3 wherein there are at least two further layers, one on each side of said narrow bandgap region.

5. A transistor according to claim 1 wherein said narrow bandgap region comprises InSb or InAs.

6. A transistor according to claim 1 wherein the transistor is a quantum-well FET.

7. A transistor according to claim 6 wherein the quantum well is provided by a primary conduction channel and at least one secondary conduction channel immediately adjacent and in contact with the primary channel, the secondary channel having an effective bandgap greater than the effective bandgap Eg (effective) of the primary channel, wherein the modulus of the difference between the effective impact ionisation threshold IIT (effective) and the effective conduction band offset ΔE_C (effective) between the primary and secondary channels being no more than 0.5 Eg (effective).

8. A transistor according to claim 7 wherein the quantum well is provided by a primary conduction channel and at least one secondary conduction channel immediately adjacent and in contact with the primary channel, the secondary channel having an effective bandgap greater than the effective bandgap Eg (effective) of the primary channel, wherein the modulus of the difference between the effective impact ionisation threshold IIT (effective) and the effective conduction band offset ΔE_C (effective) between the primary and secondary channels being no more than 0.4 eV.

9. A transistor according to claim 6 in the form of an extracting transistor characterised in that (a) it is a field effect transistor incorporating a conducting region consisting at least partly of a quantum well; (b) the quantum well is in an at

least partly intrinsic conduction regime when the transistor is unbiased and at a normal operating temperature; and (c) it includes at least one junction which is biasable to reduce the intrinsic conduction in the quantum well and confine charge carriers predominantly to one type only corresponding to an extrinsic saturated regime.

10. A transistor according to claims 1 wherein the transistor is an n-p-n bipolar transistor.

11. A transistor according to claim 10 with a vertical geometry having a base region provided with a base contact, emitter and collector regions arranged to extract minority carriers from the base region, and a structure for counteracting entry of minority carriers into the base region via the base contact, wherein the base region has a bandgap of greater than 0.5 eV and a doping level greater than 10^{17} cm^{-3}.

12. A transistor according to claim 1 wherein the narrow bandgap is no more than 1.0 eV.

13. A complementary logic circuit comprising a transistor according to claim 1.

14. An integrated circuit comprising a transistor according to claim 1.

16. A quantum-well field effect transistor including at least one narrow bandgap region or layer that is doped p-type or contains an excess of holes and is subject to compressive mechanical strain, wherein said transistor incorporating a conducting region consisting at least partly of a quantum well; (b) the quantum well is in an at least partly intrinsic conduction regime when the transistor is unbiased and at a normal operating temperature; and (c) it includes at least one junction which is biasable to reduce the intrinsic conduction in the quantum well and confine charge carriers predominantly to one type only corresponding to an extrinsic saturated regime.

X. EVIDENCE APPENDIX

Copy of GB 2 362 506 cited in the specification as evidence of well known structure.

(12) UK Patent Application (19) GB (11) 2 362 506 (13) A

(43) Date of A Publication 21.11.2001

(21) Application No 0012017.0

(22) Date of Filing 19.05.2000

(51) INT CL[7]
H01L 29/778

(52) UK CL (Edition S)
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(56) Documents Cited
GB 2266183 A EP 0460793 A1 EP 0167305 A2
Applied Physics Letters Vol.59, No.14, September 1991, T. Ashley et al "Ambient temperature diodes and field-effect transistors..." see pages 1761 - 1763

(58) Field of Search
UK CL (Edition R) H1K KFN
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Online: EPODOC, JAPIO, WPI, TXTE, INSPEC

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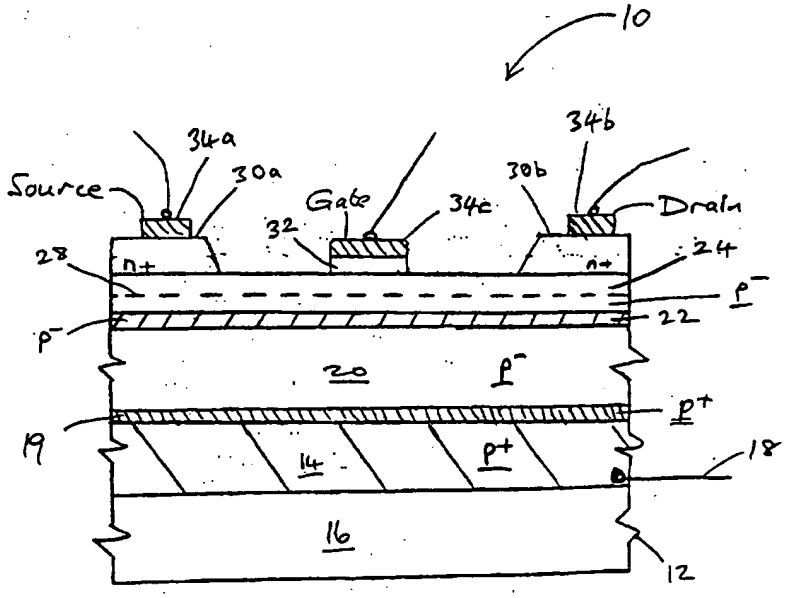
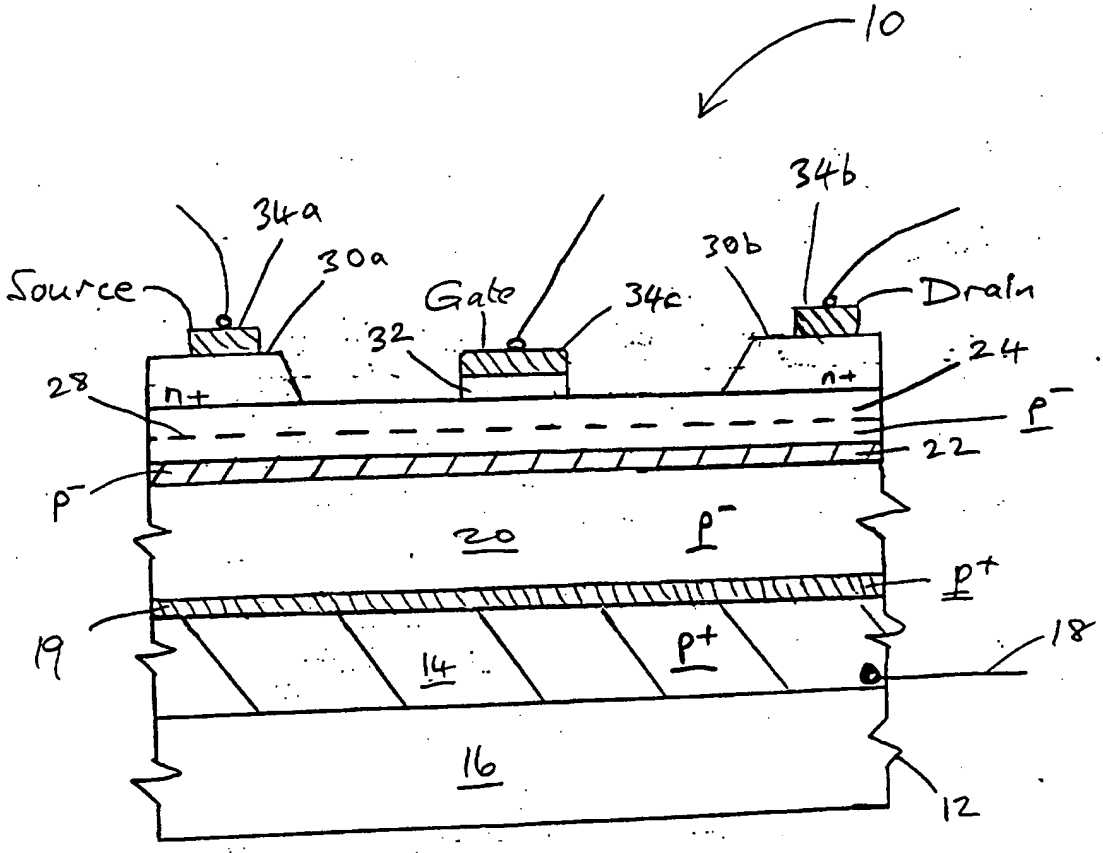
(54) Abstract Title
Field effect transistor with an InSb quantum well and minority carrier extraction

(57) A field effect transistor 10 and a method of forming said transistor comprises a quantum well 22 which is at least partially in an intrinsic conduction state when the transistor 10 is unbiased and is at a normal operating temperature. The transistor 10 includes means to bias the transistor such that charge carriers in the quantum well 22 are predominately those relating to a saturated extrinsic conduction state. The quantum well 22 may be a p-type InSb layer located between InAlSb layers 20, 24. Layer 24 may include an ultra-thin delta-doped Si layer 28 which provides a dominant source of charge carriers for the quantum well 22. Layer 20 may be formed on a barrier layer 19, a substrate layer 14 and a substrate 16. The transistor 10 may have an insulated gate electrode 34c and n^+ source and drain layers 30a, 30b and electrodes 34a, 34b which may have a positive bias relative to a substrate electrode 18 such that they can provide minority carrier extraction in the quantum well 22, reducing the intrinsic contribution to conductivity. The transistor 10 may provide a predominately saturated extrinsic conduction state with low leakage current.



GB 2 362 506 A


10
34b
34a
30b
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Source
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34c
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32
24
28
n+
n+
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p⁻
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12

EXTRACTING TRANSISTOR

This invention relates to an extracting transistor, that is to say a transistor in which intrinsic conductivity is reduced by carrier extraction.

Before considering the prior art, semiconductor nomenclature and properties will be discussed. Transistor operation relies on electrical transport effects in semiconductor material, and, broadly speaking, there are three important conduction regimes: unsaturated extrinsic, saturated extrinsic and intrinsic, and these occur at low, intermediate and high temperature respectively. In the unsaturated extrinsic regime, there is insufficient thermal energy to ionise all impurities and the carrier concentration is temperature dependent because more impurities are ionised as temperature increases. Carriers are thermally activated from dopant impurities of a single species, i.e. donors or acceptors. Conduction is due substantially to one kind of carrier in one band, i.e. electrons in the conduction band or holes in the valence band but not both. The saturated extrinsic regime is similar, but occurs at higher temperatures at which virtually all impurities have become ionised but insufficient thermal energy is available to ionise significant numbers of valence band states to create electron-hole pairs: here the carrier concentration is largely independent of temperature.

In the intrinsic regime, conduction has a substantial contribution from thermal ionisation of valence band states producing both types of carrier, i.e. electron-hole pairs, in addition to carriers of one type activated from impurities. Conduction is due to both kinds of carrier in both bands, i.e. electrons in the conduction band and holes in the valence band. Conductivity varies with temperature in this regime because the electron-hole pair concentration is temperature dependent. There is an intervening transition region between the extrinsic and intrinsic regimes where conduction is partially extrinsic and partially intrinsic giving rise to more of one type of charge carrier than the other, i.e. majority carriers and minority carriers: it is at or near ambient temperature in

Ge depending on doping. The onset temperature of intrinsic conduction depends on band

gap and dopant concentration; it can occur below ambient temperature, as low as 150K in narrow gap semiconductors with low doping.

Materials such as Si and GaAs with a saturated extrinsic regime at ambient temperature are preferred for transistor applications despite their inferior mobility properties: this is because of the need for very low intrinsic carrier concentrations in the active regions of devices. Highly pure Ge is intrinsic at ambient temperature, and by analogy with this weakly doped Si is sometimes referred to wrongly as intrinsic, such as in PIN diodes where the high resistivity I ("intrinsic") region is in fact extrinsic at ambient temperature. The purest Si currently available is more than an order of magnitude too impure to be intrinsic at ambient temperature.

Narrow band-gap semiconductors such as indium antimonide (InSb) have useful properties such as very low electron effective mass, very high electron mobility and high saturation velocity. These are potentially of great interest for ultra high speed transistor applications. InSb in particular is a promising material for fast, very low power dissipation transistors, because its electron mobility μ_e at low electric fields is nine times higher than that of GaAs and its saturation velocity v_{sat} is more than five times higher, despite GaAs having better properties than Si in these respects. InSb is also predicted to have a large ballistic mean free path of over 0.5 μm. This suggests that InSb has potential for high speed operation at very low voltages with consequent low power consumption, which would make it ideal for portable and high-density applications. Some of the properties of Silicon, GaAs and InSb at 295K (ambient temperature) are compared in Table 1 below.

Table 1: Properties of InSb at 295 K

Parameter	Silicon	GaAs	InSb	Units
E_G Band-gap	1.12	1.43	0.175	eV
m^*_e Electron Effective Mass	0.19	0.072	0.013	m_0
μ_e Electron Mobility	1,500	8,500	78,000	$cm^2 V^{-1} s^{-1}$
v_{sat} Saturation Velocity	$1'10^7$	$1'10^7$	$>5'10^7$	$cm\ s^{-1}$
l_e Electron Mean Free Path	0.04	0.15	0.58	μm
n_i Intrinsic Carrier Concentration	$1.6'10^{10}$	$1.1'10^7$	$1.9'10^{16}$	cm^{-3}

Until recently, the potentially valuable properties of InSb have been inaccessible at ambient temperatures due to its low band-gap and consequently high intrinsic carrier concentration (~$2x10^{16}$ cm^{-3}), which is six and nine orders of magnitude above those of Si and GaAs respectively. This leads to InSb devices exhibiting high leakage currents at normal operating temperatures at or near ambient temperature of 295K, where the minority carrier concentration is much greater than the required value at normal doping levels. It was thought for many years that this was a fundamental problem which debarred InSb and other narrow band-gap materials from use in devices at ambient temperature and above.

The problem was however overcome to some extent in the invention the subject of US Pat. No. 5,382,814: this patent discloses a non-equilibrium metal-insulator-semiconductor field effect transistor (MISFET) using the phenomena of carrier exclusion and extraction to reduce the intrinsic contribution to the carrier concentration below the equilibrium level. The MISFET is a reverse-biased $p^+p^+p^-n^+$ structure, where

p denotes an InSb layer, $\underline{p}$ is a strained $In_{1-x}Al_xSb$ layer (underlined $\underline{p}$ indicates wider band-gap than p), p^- indicates a weakly doped p-type region that is intrinsic at ambient operating temperature, and the + superscript indicates a high dopant concentration; these four layers define three junctions between adjacent layer pairs, i.e. $p^+\underline{p}^+$, $\underline{p}^+p^-$ and p^-n^+ junctions respectively. The active region of the device is the p^- region, and minority carriers are removed from it at the p^-n^+ junction acting as an extracting contact. The $\underline{p}^+p^-$ junction is an excluding contact which inhibits re-introduction of these carriers. In consequence, under applied bias the minority carrier concentration falls in the active region, and the majority carrier concentration falls with it to a like extent to preserve charge neutrality. This reduces electron and hole concentrations by like amounts, which corresponds to a reduction in the intrinsic contribution to conductivity (electron-hole pairs) and takes the active region into an extrinsic-like regime.

International Patent Application No. WO 99/28975 published under the Patent Cooperation Treaty relates to a similar transistor which has a straightened channel to improve frequency response. These prior art extracting devices however suffer from the problem that they exhibit relatively high leakage current which increases power requirements and operating temperature.

It is an object of the invention to provide an alternative form of extracting transistor capable of operation with lower leakage current than the prior art.

An extracting transistor characterised in that:

a) it is a field effect transistor incorporating a conducting region consisting at least partly of a quantum well;

b) the quantum well is in an at least partially intrinsic conduction regime when the transistor is unbiased and at a normal operating temperature; and

c) it includes at least one junction which is biasable to reduce intrinsic conduction in the quantum well and confine charge carriers predominantly to one type only corresponding to an extrinsic saturated regime.

The invention provides the advantage that with transistor design in accordance with ordinary skill in the art of semiconductor device fabrication it is capable of reducing leakage current considerably: examples of the invention have exhibited an order of magnitude reduction leakage current.

The transistor of the invention may contain an excluding junction for inhibiting minority carrier supply to the quantum well; it may be arranged for carrier exclusion at least partly by incorporation of an excluding heterojunction between two semiconductor materials of differing band-gap both wider than that of the quantum well.

The biasable junction may be an extracting junction for removal of carriers from the quantum well. It may be a heterojunction between indium antimonide and a semiconductor material having a wider band gap than indium antimonide: e.g. indium aluminium antimonide with x is in the range 0.10 to 0.5, preferably 0.15 to 0.2 or substantially 0.15.

The excluding junction may be a heterojunction between indium antimonide and a semiconductor material having a wider band gap than indium antimonide.

The quantum well material may have a band gap less than 0.4 eV, and may be indium antimonide.

In a preferred embodiment, the transistor of the invention includes a δ-doping layer arranged to be a dominant source of charge carriers for the quantum well. It may have an n^+-p^- - quantum well - p^--p^+-p^+ diode structure or an n^+-p^- - quantum well - p^--p^+ diode structure.

The transistor of the invention may include a first excluding junction for inhibiting minority carrier supply to the quantum well and wide band-gap barrier layer to enhance

such inhibiting effect. It may include a gate contact insulated from the active region by insulating material such as silicon dioxide or wide band-gap semiconductor material.

The transistor may alternatively include a gate contact deposited directly upon a surface of the active region and forming a Schottky contact thereto.

In one embodiment, the transistor includes source, gate and drain electrodes and a substrate contact, the biasable junction is a pn junction reverse biasable via the substrate contact to produce minority carrier extraction from the quantum well, and the substrate contact is connected externally to the source electrode.

The transistor may be p-channel with a p^+-$\underline{n}^-$-quantum well - $\underline{n}^-$-$\underline{\underline{n}}^+$-$\underline{n}^+$ or a p^+-$\underline{p}^-$-quantum well - $\underline{p}^-$-$\underline{\underline{n}}^+$-$n^+$ structure, and include a δ-doping layer providing a predominant source of holes for the active region.

In another aspect, the invention provides a method of obtaining transistor operation characterised in that it includes the steps of:

a) providing an extracting field effect transistor incorporating:

i) source, gate and drain electrodes and a substrate contact and between such electrodes and contact a pn junction biasable via the substrate contact for minority carrier extraction;

ii) a conducting region consisting at least partly of a quantum well in an at least partially intrinsic conduction regime when the transistor is unbiased and at a normal operating temperature; and

iii) at least one junction which is biasable to reduce intrinsic conduction in the quantum well and confine charge carriers predominantly to one type only corresponding to an extrinsic saturated regime;

b) biasing the substrate contact to reverse bias the pn junction and to arrange for the substrate contact either to be at the same potential as the source

electrode, or to be negative or positive with respect to the source electrode according to whether such electrode is associated with a p-type or n-type component of the pn junction.

In order that the invention might be more fully understood, an embodiment thereof will now be described, by way of example only, with reference to the accompanying single figure drawing, which is a schematic vertical sectional view of an extracting transistor of the invention.

Referring to the drawing, an extracting, depletion mode, field effect transistor (FET) 10 is shown, but as indicated by zigzag lines such as 12 it is not drawn to scale. The FET 10 incorporates a 1 μm thick substrate layer 14 of $\underline{p}^+$-type $In_{0.85}Al_{0.15}Sb$ with a high dopant concentration of $2x10^{18}$ cm^{-3} upon an insulating substrate 16 of GaAs and having an electrical bias contact 18, which optionally may be relocated more remotely. The layer 14 bears an optional 20 nm thick barrier layer 19 of $\underline{\underline{p}}^+$-type $In_{0.7}Al_{0.3}Sb$ with a high dopant concentration $2x10^{18}$ cm^{-3}: here double underlining of $\underline{\underline{p}}^+$ indicates wider band-gap than $\underline{p}^+$, which in turn (as has been said) indicates wider band-gap than p. The barrier layer 19 is surmounted by an 0.5 μm thick layer 20 of $\underline{p}^-$-type $In_{0.85}Al_{0.15}Sb$ which is doped at less than $3x10^{16}$ cm^{-3}.

Upon the layer 20 there is a 15 nm thick quantum well 22 of p^--type InSb with a dopant concentration of less than $3x10^{16}$ cm^{-3}. The quantum well 22 is in turn surmounted by a 150 nm thick layer 24 (acceptable thickness range 100-200 nm): the latter consists largely of less than $3x10^{16}$ cm^{-3} $\underline{p}^-$-type $In_{0.85}Al_{0.15}Sb$; it incorporates an ultra-thin silicon n-type δ-doping layer 28. The δ-doping layer 28 is indicated by a chain line and is spaced apart from the quantum well 22 by a distance in the range 10-40 nm. It provides a two-dimensional electron gas with concentration per unit area in the range $6x10^{11}$ cm^{-2} to $2x10^{12}$ cm^{-2}, e.g. $1x10^{12}$ cm^{-2}: the gas forms in the quantum well 22 because it is energetically favourable - this is referred to as modulation doping, and the electron gas

concentration remains substantially independent of temperature because it is a function of dopant concentration only.

The layer 24 has deposited upon it two outer n+ contact regions 30a and 30b of InSb 30 nm thick and a central insulator layer 32, and the latter 30a, 30b and 32 are in turn surmounted. by respective metal layers 34a, 34b and 34c (collectively 34). The insulator layer 32 may be silicon dioxide or a semiconductor material of wider band-gap than that of InSb. The metal layers 34 are electrical connections and act respectively as FET source and drain electrodes for the FET 10. The n+ contact regions 30a and 30b are separated by a distance in the range 0.5 to 2 μm, e.g. 1 μm.

The FET 10 is an n^+-p^--quantum well - p^--p^+-p^+ diode structure in which the quantum well 22 undergoes carrier extraction when a reverse bias is applied, i.e. with one or both of the source and drain electrodes 34a and 34b biased positive with respect to the substrate layer contact 18. This is because the interfaces between layer 24 and each of layers 30a/30b is an n^+p^- junction which is an extracting contact when reverse biased. The carrier concentration in the quantum well 22 is reduced by bias to considerably below the intrinsic equivalent which prevails in the absence of bias, and here again it becomes largely independent of temperature simulating a saturated extrinsic regime: this provides a low leakage current between source 34a and drain 34b when negative bias is applied to the gate 34c to turn off the FET 10. Electrons from the δ-doping layer 28 are then the dominant source of charge carriers in the quantum well 22. The FET active region, i.e. the gate-controlled conducting channel between contact layers 30a and 30b is largely that in the quantum well 22. Layers 14, 19, 20 and 24 of the FET 10 have much wider band-gap than the quantum well 22 and the leakage current contributions from these regions can be ignored.

The principle of carrier extraction is known in the prior art and is described in for example European Patent No EP 0167305 and US Patent No 5,016,073. It involves removing minority carriers from a semiconductor region at a greater rate than they are replaced; it occurs at a biased pn junction 24/30 to which minority carriers diffuse and

over which they are swept by its potential drop - i.e. at which they are extracted and become lost to the region. These carriers (electrons in this case) cannot be replenished in the quantum well 22 because the only available source is the p^- layer 20 which has an inadequate (negligible) concentration of them: i.e. the p^-p^- junction between layers 20 and 22 and the p^+p^- junction between layers 19 and 20 are what is referred to as excluding contacts which inhibit minority carriers reaching the quantum well 22.

In the FET 10 the carrier concentration in the quantum well (22) is kept low and temperature independent: this makes it more suitable than prior art devices for demanding applications. It performs well in this regard because the quantum well carrier concentration is very largely determined by modulation doping, which is a temperature-independent parameter unlike thermal activation of electron-hole pairs. The FET's off-state drain leakage current under bias (i.e. source-drain current with gate biased to cut-off) is at least an order of magnitude lower than comparable prior art devices.

By virtue of the gate insulation layer 32, the FET 10 is a metal-insulator-semiconductor device, i.e. a MISFET. It is possible to dispense with the insulation layer 32, which would make the gate electrode 34c a Schottky contact to the p^- layer 24. In this Schottky case the FET transconductance is about 3-4 times higher than that of a comparable prior art device with a typical gate oxide thickness of around 30 – 70 nm. Output conductance is typically half that of comparable prior art devices the subject of US Pat. No. 5,382,814 and International Patent Application No. WO 99/28975 published under the Patent Cooperation Treaty. These properties are obtained largely as a result of the preponderance of wide band-gap semiconductor material in the FET 10: such material gives low leakage current and confinement of carriers in the quantum well 22 providing good transistor action i.e. high gain and low output conductance.

The barrier layer 19 is also optional because the FET 10 is viable without it: it is intended to provide lower off-state leakage current by providing more efficient carrier exclusion, but it is not known how significant this effect is. It provides an excluding junction between layers 19 and 20 additional to that between layers 20 and 22: this

additional junction is a heterojunction between two semiconductor materials of like conductivity type (p-type) but differing band-gap both larger than that of indium antimonide.

The FET 10 may be operated with the substrate layer contact 18 reverse biased with respect to the source electrode 34a, or with the contact 18 and electrode 34a at the same potential, or with these shorted together. Since the FET 10 is largely p-type with n-type layers 30a and 30b, a reverse biased substrate layer contact 18 is negatively biased with respect to the source electrode 34a; for an equivalent FET of reversed layer conductivity type, i.e. p-type contact layers equivalent to layers 30a and 30b and other layers n-type, a reverse biased substrate layer contact 18 would be positively biased with respect to a source electrode; i.e. the substrate layer contact 18 is positive or negative with respect to the source electrode (34a) according to whether such electrode is associated with a n-type or p-type component (30a) of the extracting pn junction (24/30).

The FET 10 is an n-channel device because electrons provide conduction in the quantum well 22. A p-channel equivalent is formed by changing each layer 14/19/20/22/24/30 in the FET 10 to its respective opposite conductivity type: i.e. the n^+-$\underline{p}^-$-quantum well - $\underline{p}^-$-$\underline{\underline{p}}^+$-$\underline{p}^+$ structure becomes a p^+-$\underline{n}^-$-quantum well - $\underline{n}^-$-$\underline{\underline{n}}^+$-$\underline{n}^+$ structure with a δ-doping layer of berylllium providing a predominant source of holes for the quantum well equivalent of layer 22. It is not in fact essential to change the conductivity types of the equivalents of the quantum well and its adjacent layers, i.e. layers 22, 20 and 24: these have low dopant concentrations and therefore do not greatly affect device operation; if they are not changed the resulting structure is p^+-$\underline{p}^-$-quantum well - $\underline{p}^-$-$\underline{\underline{n}}^+$-$n^+$. Either of these p-channel devices may be advantageous because each contains a strained quantum well equivalent to layer 22, and such a well is believed to raise hole mobility due to more light hole transport.

CLAIMS

1. An extracting transistor characterised in that:
   a) it is a field effect transistor (10) incorporating a conducting region (20, 22, 24) consisting at least partly of a quantum well (22);
   b) the quantum well (22) is in an at least partially intrinsic conduction regime when the transistor (10) is unbiased and at a normal operating temperature; and
   c) it includes at least one junction (24/30) which is biasable to reduce intrinsic conduction in the quantum well (22) and confine charge carriers predominantly to one type only corresponding to an extrinsic saturated regime.

2. A transistor according to Claim 1 characterised in that it contains an excluding junction (20/22) for inhibiting minority carrier supply to the quantum well (22).

3. A transistor according to Claim 1 or 2 characterised in that it is arranged for carrier exclusion at least partly by incorporation of an excluding heterojunction (19/20) between two semiconductor materials of differing band-gap both wider than that of the quantum well (22).

4. A transistor according to Claim 1 characterised in that the biasable junction is an extracting junction (24/30a, 24/30b) for removal of carriers from the quantum well (22).

5. A transistor according to Claim 4 characterised in that the extracting junction (24/30) is a heterojunction between indium antimonide (30) and a semiconductor material (24) having a wider band gap than indium antimonide.

6. A transistor according to Claim 5 characterised in that the wider band gap material (24) is an indium aluminium antimonide material.

7. A transistor according to Claim 6 characterised in that the indium aluminium antimonide material is $In_{1-x}Al_xSb$ where x is in the range 0.10 to 0.5.

8. A transistor according to Claim 7 characterised in that x is in the range 0.15 to 0.2.

9. A transistor according to Claim 8 characterised in that x is substantially 0.15.

10. A transistor according to Claim 1 characterised in that the quantum well (22) material has a band gap less than 0.4 eV.

11. A transistor according to Claim 1 characterised in that the quantum well (22) is of indium antimonide material.

12. A transistor according to any preceding claim characterised in that it includes a δ-doping layer arranged to be a dominant source of charge carriers for the quantum well (22).

13. A transistor according to any preceding claim characterised in that it has an n^+-p^- - quantum well - p^--p^+-p^+ diode structure.

14. A transistor according to any preceding claim characterised in that it has an n^+-p^- - quantum well - p^--p^+ diode structure.

15. A transistor according to Claim 1 characterised in that it includes a first excluding junction (20/22) for inhibiting minority carrier supply to the quantum well (22) and a wide band-gap barrier layer (19) to enhance such inhibiting effect

16. A transistor according to any preceding claim characterised in that it includes a gate contact (34c) insulated from the active region (24) by insulating material (32).

17. A transistor according to Claim 16 where the insulating material (32) is silicon dioxide.

18. A transistor according to any one of Claims 1 to 15 characterised in that it includes a gate contact (34c) separated from the active region (22, 24) by semiconductor material (32) of wider band-gap than that of region 24.

19. A transistor according to any one of Claims 1 to 15 characterised in that it includes a gate contact deposited directly upon a surface of the active region (22, 24) and forming a Schottky contact thereto.

20. A transistor according to Claim 1 characterised in that it includes source, gate and drain electrodes (34) and a substrate contact (18), the biasable junction is a pn junction (24/30) reverse biasable via the substrate contact (18) to produce minority carrier extraction from the quantum well (22), and the substrate contact (18) is connected to the source electrode (34a).

21. A transistor according to Claim 1 characterised in that it is a p-channel transistor.

22. A transistor according to Claim 21 characterised in that it is a p^+-$\underline{n}^-$-quantum well - $\underline{\underline{n}}^-$-$\underline{\underline{n}}^+$-$\underline{n}^+$ structure with a δ-doping layer providing a predominant source of holes for the active region.

23. A transistor according to Claim 21 characterised in that it is a p^+-$\underline{p}^-$-quantum well - $\underline{p}^-$-$\underline{\underline{n}}^+$-$n^+$ structure with a δ-doping layer providing a predominant source of holes for the active region.

24. A method of obtaining transistor operation characterised in that it includes the steps of:

a) providing an extracting field effect transistor (10) incorporating

i) source, gate and drain electrodes (34) and a substrate contact (18) and between such electrodes and contact a pn junction (24/30) biasable via the substrate contact (18) for minority carrier extraction;

ii) a conducting region (20, 22, 24) consisting at least partly of a quantum well (22) in an at least partially intrinsic conduction regime when the transistor (10) is unbiased and at a normal operating temperature; and

iii) at least one junction (24/30) which is biasable to reduce intrinsic conduction in the quantum well (22) and confine charge carriers predominantly to one type only corresponding to an extrinsic saturated regime;

b) biasing the substrate contact (18) to reverse bias the pn junction (24/30) and to arrange for the substrate contact (18) either to be at the same potential as the source electrode (34a), or to be positive or negative with respect to the source electrode (34a) according to whether such electrode is associated with a n-type or p-type component (30a) of the pn junction (24/30).

Application No: GB 0012017.0
Claims searched: 1 - 24

Examiner: John Watt
Date of search: 1 November 2000

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Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.R): H1K (KFN)

Int Cl (Ed.7): H01L 29/10, 29/778

Other: Online: EPODOC, JAPIO, WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A	GB 2266183 A	(SECRETARY OF STATE FOR DEFENCE) see page 1,line 24 to page 4, line 7	1
A	EP0460793 A1	(AT&T) see figs.1 - 4 and page 4, lines 14, 15	1
A	EP 0167305 A2	(SECRETARY OF STATE FOR DEFENCE) see page 2, line 1 - 34	1
A	Applied Physics Letters Vol.59, No.14, September 1991, T. Ashley et al "Ambient temperature diodes and field-effect transistors in InSb/In1-x AlxSb" see pages 1761-1763		1

X Document indicating lack of novelty or inventive step
Y Document indicating lack of inventive step if combined with one or more other documents of same category.
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P Document published on or after the declared priority date but before the filing date of this invention.
E Patent document published on or after, but with priority date earlier than, the filing date of this application.

XI. RELATED PROCEEDINGS APPENDIX

None.